

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Richard Hsiao et al.

Application No.: 10/717,112

Group No.: 2627

Filed: November 19, 2003

Examiner: Klimowicz, William J.

For: MAGNETIC HEAD COIL STRUCTURE AND METHOD FOR MANUFACTURING THE SAME

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

DECLARATION OF PRIOR INVENTION IN THE UNITED STATES  
OR IN A NAFTA OR WTO MEMBER COUNTRY  
TO OVERCOME CITED PATENT OR PUBLICATION (37 C.F.R. § 1.131)

PURPOSE OF DECLARATION

1. This declaration is to establish completion of the invention of claims 1 and 20 of this application in the United States at a date prior to March 14, 2002, that is the effective 102(a) date of the prior art publication that was cited by the Examiner.
2. The person making this declaration are the inventors.

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**CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10\***

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I hereby certify that, on the date shown below, this correspondence is being:

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**TRANSMISSION**

, facsimile transmitted to the Patent and Trademark Office, (703) \_\_\_\_\_

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(type or print name of person certifying)

\* Only the date of filing (§ 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under § 1.8 continues to be taken into account in determining timeliness. See § 1.703(f). Consider "Express Mail Post Office to Addressee" (§ 1.10) or facsimile transmission (§ 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.

### FACTS AND DOCUMENTARY EVIDENCE

3. As evidence of the date of conception of the invention of this application, the following attached documents and/or models are submitted as evidence:

STATEMENT: I hereby state that conception of the invention of claims 1 and 20 in the above-identified patent application were made prior to March 14, 2002, as supported by Exhibit A. Exhibit A, dated November 15, 2001, shows the pertinent portions of a draft of the present application faxed to the inventors. I state that the concepts and features described in Exhibit A were conceived, and documented by the inventor prior to March 14, 2002.

EXHIBIT A: Copy of a draft of the present application dated November 15, 2001.

Exhibit A demonstrates that the subject matter of claims 1 and 20 (as amended) were in the inventors' possession at least as early as November 15, 2001 as described below.

Page 1 of the facsimile, the fax cover sheet, discloses the date of the facsimile to the inventors (see "Date: November 15, 2001 and timestamp/page stamp on bottom of page).

Page 10, 11, 15, 20, and page 30 of the facsimile, disclose claim 1:

A magnetic head coil structure, comprising:

an insulating layer (see item 402 of Figure 4A, and Page 10 of facsimile, lines 21-22);

a photoresist layer deposited on the insulating layer (see item 404 of Figure 4A, and Page 11 of facsimile, line 3);

a silicon dielectric layer deposited on the photoresist layer (see item 406 of Figure 4A, and Page 11 of facsimile, lines 9-10), the silicon dielectric layer having at least one channel formed therein (see item 412 of Figure 4B, and Page 11 of facsimile, lines 18-20);

a conductive material formed in the at least one channel to define a coil structure (see item 414 of Figure 4C, and Page 15 of facsimile, lines 1-2);

wherein a grain size of the conductive material is less than half of a smallest dimension of the at least one channel (see claim 5 of Page 20).

Page 19 and page 20 of the facsimile, disclose claim 20:

A magnetic head coil structure manufactured utilizing a process, comprising:

depositing an insulating layer;  
depositing a photoresist layer on the insulating layer;  
depositing a silicon dielectric layer on the photoresist layer;  
masking the silicon dielectric layer;  
etching at least one channel in the photoresist layer and the silicon dielectric layer;  
depositing a conductive seed layer in the at least one channel; and  
filling the at least one channel with a conductive material to define a coil structure (see  
Page 19 of facsimile, lines 1-9 of claim 1);  
wherein a grain size of the conductive material is less than half of a smallest dimension of  
the at least one channel (see Page 20 of facsimile, claim 5).

#### **DILIGENCE**

4. It is hereby declared that Applicants acted diligently up to reduction of practice or the filing date of the present patent application.

#### **TIME OF PRESENTATION OF THE DECLARATION**

5. This declaration is submitted prior to final rejection, or with a first or supplementary first reply after a final rejection for the purpose of overcoming a new ground of rejection or requirement made by the examiner, in which case the declaration is considered timely and should be considered. See MPEP 715.09(c).

#### **DECLARATION**

6. As a person signing below:

I hereby declare that the documents attached hereto disclose the subject matter of currently pending claims 1 and 20 of the subject patent application. I also declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

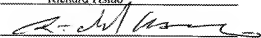
#### **SIGNATURE(S)**

Typewritten Full Name of  
Sole or First Inventor:

Richard Hsiao

Citizenship: USA

Inventor's signature:



Date of Signature: \_\_\_\_\_

Residence: (City) San Jose

(State/Country) CA /USA

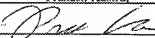
Post Office Address: 6601 Neptune Court, San Jose, California 95120

Typewritten Full Name of  
Second or Joint Inventor:

Prakash Kasiraj

Citizenship: USA

Inventor's signature:



Date of Signature: 7/9/07

Residence: (City) San Jose

(State/Country) CA /USA

Post Office Address: 790 Finchwood Way, San Jose, California 95120

Typewritten Full Name of  
Third or Joint Inventor:

Quang Le

Citizenship: USA

Inventor's signature:

\_\_\_\_\_

Date of Signature: \_\_\_\_\_

Residence: (City) San Jose

(State/Country) CA /USA

Post Office Address: 3365 Vangorn Way, San Jose, California 95121

Typewritten Full Name of  
Fourth or Joint Inventor:

Paul Phong Nguyen

Citizenship: USA

Inventor's signature:

\_\_\_\_\_

Date of Signature: \_\_\_\_\_

Residence: (City) San Jose

(State/Country) CA /USA

Post Office Address: 233 Blossom Hill Road, #D8, San Jose, California 95123

Typewritten Full Name of  
Fifth or First Inventor:

Son Van Nguyen

Citizenship: USA

Inventor's signature:

\_\_\_\_\_

Date of Signature: \_\_\_\_\_

Residence: (City) Los Gatos

(State/Country) CA /USA

Post Office Address: 16075 Blossom Hill Road, Los Gatos, California 95032

Typewritten Full Name of  
Sixth or Joint Inventor:

Denny D. Tang

Citizenship: USA

Inventor's signature:

\_\_\_\_\_

Date of Signature: \_\_\_\_\_

Typewritten Full Name of  
Sole or First Inventor: Richard Hsiao Citizenship: USA

Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_

Residence: (City) San Jose (State/Country) CA /USA

Post Office Address: 6601 Neptune Court, San Jose, California 95120

Typewritten Full Name of  
Second or Joint Inventor: Prakash Kastraj Citizenship: USA

Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_

Residence: (City) San Jose (State/Country) CA /USA

Post Office Address: 790 Finchwood Way, San Jose, California 95120

Typewritten Full Name of  
Third or Joint Inventor: Quang Le Citizenship: USA

Inventor's signature:  Date of Signature: 7/10/07

Residence: (City) San Jose (State/Country) CA /USA BLC

Post Office Address: 3365 Vainhorn Way, San Jose, California 95121 3257 Capriana Cir., San Jose CA 95135

Typewritten Full Name of  
Fourth or Joint Inventor: Paul Phong Nguyen Citizenship: USA

Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_

Residence: (City) San Jose (State/Country) CA /USA

Post Office Address: 233 Blossom Hill Road, #D8, San Jose, California 95123

Typewritten Full Name of  
Fifth or First Inventor: Son Van Nguyen Citizenship: USA

Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_

Residence: (City) Los Gatos (State/Country) CA /USA

Post Office Address: 16075 Blossom Hill Road, Los Gatos, California 95032

Typewritten Full Name of  
Sixth or Joint Inventor: Denny D. Tang Citizenship: USA

Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_

Declaration of Prior Invention in the United States or in a NAFTA or WTO Member Country to Overcome Cited Patent or Publication--  
37 C.F.R. section 1.131--page 4 of 6

Typewritten Full Name of  
Sole or First Inventor: Richard Hsiao Citizenship: USA  
Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_  
Residence: (City) San Jose (State/Country) CA /USA  
Post Office Address: 6601 Neptune Court, San Jose, California 95120

Typewritten Full Name of  
Second or Joint Inventor: Prakash Kasiraj Citizenship: USA  
Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_  
Residence: (City) San Jose (State/Country) CA /USA  
Post Office Address: 790 Finchwood Way, San Jose, California 95120

Typewritten Full Name of  
Third or Joint Inventor: Quang Le Citizenship: USA  
Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_  
Residence: (City) San Jose (State/Country) CA /USA  
Post Office Address: 3365 Vangorn Way, San Jose, California 95121

Typewritten Full Name of  
Fourth or Joint Inventor: Paul Phong Nguyen Citizenship: USA  
Inventor's signature: Paul Phong Nguyen Date of Signature: 6/18/2007  
Residence: (City) San Jose (State/Country) CA /USA  
Post Office Address: 233 Blossom Hill Road, #D8, San Jose, California 95125

1764 Chevalier Dr., San Jose, California 95124  
P.N.  
Typewritten Full Name of  
Fifth or First Inventor: Son Van Nguyen Citizenship: USA  
Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_  
Residence: (City) Los Gatos (State/Country) CA /USA  
Post Office Address: 16075 Blossom Hill Road, Los Gatos, California 95032

Typewritten Full Name of  
Sixth or Joint Inventor: Denny D. Tang Citizenship: USA  
Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_

Typewritten Full Name of  
Sole or First Inventor:

Richard Hsiao

Citizenship: USA

Inventor's signature: \_\_\_\_\_

Date of Signature: \_\_\_\_\_

Residence: (City)

San Jose

(State/Country) CA /USA

Post Office Address:

6601 Neptune Court, San Jose, California 95120

Typewritten Full Name of  
Second or Joint Inventor:

Prakash Kasiraj

Citizenship: USA

Inventor's signature: \_\_\_\_\_

Date of Signature: \_\_\_\_\_

Residence: (City)

San Jose

(State/Country) CA /USA

Post Office Address:

790 Finchwood Way, San Jose, California 95120

Typewritten Full Name of  
Third or Joint Inventor:

Quang Le

Citizenship: USA

Inventor's signature: \_\_\_\_\_

Date of Signature: \_\_\_\_\_

Residence: (City)

San Jose

(State/Country) CA /USA

Post Office Address:

3365 Vangorn Way, San Jose, California 95121

Typewritten Full Name of  
Fourth or Joint Inventor:

Paul Phong Nguyen

Citizenship: USA

Inventor's signature: \_\_\_\_\_

Date of Signature: \_\_\_\_\_

Residence: (City)

San Jose

(State/Country) CA /USA

Post Office Address:

233 Blossom Hill Road, #D8, San Jose, California 95123

Typewritten Full Name of  
Fifth or First Inventor:

Son Van Nguyen

Citizenship: USA

Inventor's signature: \_\_\_\_\_

Date of Signature: 6/18/2007

Residence: (City)

Los Gatos

Schenectady

(State/Country) NY CA /USA

Post Office Address:

16975 Blossom Hill Road, Los Gatos, California 95032

Su1

322 PARKVIEW DR, SCHENECTADY, NY 12303

Typewritten Full Name of  
Sixth or Joint Inventor:

Denny D. Tang

Citizenship: USA

Inventor's signature: \_\_\_\_\_

Date of Signature: \_\_\_\_\_

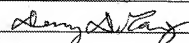
Typewritten Full Name of  
Sole or First Inventor: Richard Hsiao Citizenship: USA  
Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_  
Residence: (City) San Jose (State/Country) CA /USA  
Post Office Address: 6601 Neptune Court, San Jose, California 95120

Typewritten Full Name of  
Second or Joint Inventor: Prakash Kasiraj Citizenship: USA  
Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_  
Residence: (City) San Jose (State/Country) CA /USA  
Post Office Address: 790 Finchwood Way, San Jose, California 95120

Typewritten Full Name of  
Third or Joint Inventor: Quang Le Citizenship: USA  
Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_  
Residence: (City) San Jose (State/Country) CA /USA  
Post Office Address: 3365 Vangorn Way, San Jose, California 95121

Typewritten Full Name of  
Fourth or Joint Inventor: Paul Phong Nguyen Citizenship: USA  
Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_  
Residence: (City) San Jose (State/Country) CA /USA  
Post Office Address: 233 Blossom Hill Road, #D8, San Jose, California 95123

Typewritten Full Name of  
Fifth or First Inventor: Son Van Nguyen Citizenship: USA  
Inventor's signature: \_\_\_\_\_ Date of Signature: \_\_\_\_\_  
Residence: (City) Los Gatos (State/Country) CA /USA  
Post Office Address: 16075 Blossom Hill Road, Los Gatos, California 95032

Typewritten Full Name of  
Sixth or Joint Inventor: Denny D. Tang Citizenship: USA  
Inventor's signature:  Date of Signature June 18 2007



Residence: (City) Saratoga (State/Country) CA /USA

Post Office Address: 20407 Cunningham Place, Saratoga, California 95070

Typewritten Full Name of

Seventh or Joint Inventor: Patrick Rush Webb Citizenship: USA

Inventor's signature:  Date of Signature: 6/28/07

Residence: (City) San Jose (State/Country) CA /USA

Post Office Address: 4501 Snell Ave. #2002, San Jose, California 95136

## **EXHIBIT A**

See attached.

# SILICON VALLEY IP GROUP

303 ALMADEN BLVD., #600  
 SAN JOSE, CA 95110

TELEPHONE (408) 971-2573  
 FAX (408) 971-4660

## FAX COVER SHEET

|                         |              |            |
|-------------------------|--------------|------------|
| Date: November 15, 2001 | Phone Number | Fax Number |
| To: Son Van Nguyen, IBM |              | 927-3010   |
| From: Kevin Zilka       |              |            |

Docket No.: SJ09-2001-0089US1/IBM1P005

Total Number of Pages Being Transmitted, Including Cover Sheet:

Message:

Son,

Per your request the following is the final draft of the patent application entitled "Magnetic Head Coil Structure and Method for Manufacturing the Same".

If you have any questions please do not hesitate to contact me.

Thank you,

Kevin J. Zilka

☐ Original to follow Via Regular Mail ☒ Original will Not be Sent ☐ Original will follow Via Overnight Courier

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U.S. PATENT APPLICATION  
FOR A  
MAGNETIC HEAD COIL STRUCTURE AND  
METHOD FOR MANUFACTURING THE SAME

INVENTOR(S):  
Son Nguyen  
Quang Le  
Denny Tang  
Prakash Kasiraj  
Paul Nguyen  
Richard Hsiao  
Patrick Webb

ASSIGNEE: INTERNATIONAL BUSINESS MACHINES

KEVIN J. ZILKA  
PATENT AGENT  
P.O. Box 721120  
SAN JOSE, CA 95172

FIG. 4 illustrates a Damascene process 450 for manufacturing a coil structure for a magnetic head, in accordance with one embodiment. In such embodiment, an insulating layer is initially deposited after which a photoresist layer is deposited. Note operations 452 and 454.

- 5       Next, a silicon dielectric layer is deposited on the photoresist layer. See operation 456. Then, an adhesion promoter layer is optionally deposited in operation 458.

- After applying a masked second photoresist layer on the adhesion promoter layer in operation 460, a plurality of channels are etched in the adhesion promoter layer, the silicon dielectric layer, and the initial photoresist layer. See operation 462. Preferably,  
10   high density plasma reactive ion etching (RIE) is utilized. It should be noted that an aspect ratio of the channels is at least 7 due to the use of the silicon dielectric layer.

- Then, in operation 464, a conductive seed layer is deposited in the channels. The channels are then filled with a conductive material to define a coil structure. Note operation 466. The silicon dielectric layer, the adhesion promoter layer and portions of  
15   the conductive material are then removed using chemical-mechanical polishing (CMP). See operation 468. The coil structure may then be processed further in a manner that makes the same suitable for use with a magnetic head. FIGs. 4A-4E illustrate the various operations set forth in the process of FIG. 4 in greater detail.

- FIG. 4A illustrates a cross-sectional view of a stack 400 of materials with which  
20   the coil structure of the present embodiment is constructed. In the context of the process 450 of FIG. 4, the stack 400 is generated during operations 452-460. As shown, the stack 400 includes an insulating layer 402. In one embodiment, the insulating layer 402 may

include a plurality of sublayers including  $\text{Al}_2\text{O}_3$  /  $\text{TiC}$  ( $\text{N}_{38}$ ) or any other desired materials.

- Deposited on the insulating layer 402 is a first photoresist layer 404. In one embodiment, the first photoresist layer 404 may include AZ 1529 with a thickness of 1.9-4.0  $\mu\text{m}$ . In the prior art, performing the standard process of ion milling to remove the seed layer to form isolating Cu lines/structure on just this first photoresist layer 404 often resulted in deficient aspect ratios.

- To overcome the deficiencies of the prior art and improve the aspect ratios of a resultant coil structure, a silicon dielectric layer 406 is deposited on the first photoresist layer 404. In one embodiment, the silicon dielectric layer 406 may include  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$  or any other desired silicon dielectric material that is capable of effecting higher aspect ratios in the manner to be set forth. Further, the thickness of the silicon dielectric layer 406 may be substantially 150 nm, or above or lower than such figure.

- As an option, an adhesion promoter layer 408 may be deposited on the silicon dielectric layer 406. In one embodiment, the adhesion promoter layer 408 may include Hexamethyl Disilazane (HMDS) with a thickness of 0.5-5 nm.

- Such adhesion promoter layer 408 receives a patterned second photoresist layer 410 thereon which defines a mask. The patterned second photoresist layer 410 defines a plurality of channels 412 which, in turn, will define the resultant coil structure, as will soon become apparent. In one embodiment, the second photoresist layer 410 may include AZ 7905 with a thickness of 0.5  $\mu\text{m}$ . Further, the channels may have an opening width of 0.10-0.5  $\mu\text{m}$  or smaller.

|                                |                         |
|--------------------------------|-------------------------|
| Base Layer                     | 2.2-5 um                |
| Gas                            | 30 sccm CO <sub>2</sub> |
| Coil Power                     | 300W                    |
| Platen Power                   | 150W                    |
| Voltage Bias                   | 310V                    |
| Temperature                    | -20C                    |
| Wall Profile                   | Straight                |
| Al <sub>2</sub> O <sub>3</sub> | Sputter Minimal         |

In one embodiment, the reactive ion milling defines side walls of the channels 412 such that the slope thereof is less than one (1) and greater than zero (0) for reasons that will soon become apparent. FIG. 4B-1 is a close-up view of the encircled area of FIG. 4B showing the slope of the side walls of the channels 412. As shown, each of the side walls taper inwardly from a top to a bottom of the channels 412.

FIG. 4C shows the manner in which the channels 412 are filled with a seed layer 411, in accordance with operation 464 of FIG. 4. In one embodiment, the conductive seed layer 411 may include Cu, TaN<sub>x</sub>, Ta, or any other desired material. As an option, bright Cu may be used for reasons that will soon become apparent. By depositing the conductive seed layer after etching, the Damascene process 450 avoids the need to remove a seed layer as is required in the prior art. See again FIGS. 1-2.

As an option, the resistivity of the seed layer 411 may be specified to be less than or equal to 8.3 micro-ohm/cm in order to facilitate the deposition of the seed layer 411 in

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the channels 412. Further, the average grain size of the conductive layer 414 may be specified to be less than or equal to half of the smallest dimension of the channels. FIG. 4C-1 is a close-up view of the grain size of the seed layer 411, as shown in the encircled area of FIG. 4C.

5 In use, the smaller grain size 420 of the conductive layer 414 material may be more easily deposited down the sloped side walls of the channels 412. By this design, the sloped side walls of the channels 412, the smaller grain size of the conductive layer 414, and the low resistivity of the seed layer 411 ( $\leq 8.3$  micro-ohm/cm) work together to provide a more complete fill of the channels 412.

10 It should be noted that the seed layer 411 is deposited over an entirety of the stack 400. Note FIG. 4C. As will become apparent, this is important for affording a coil structure with optimal planarity. FIG. 4C-2 illustrates a coil structure 422 constructed utilizing a large grain size which in turn causes a coil bending defect 423. FIG. 4C-3 illustrates a coil structure 422 constructed utilizing a small grain size which avoids the  
15 coil bending defect.

FIG. 4D shows the manner in which the channels 412 are filled with a conductive material 414. Note operation 466 of FIG. 4. Ideally, both the conductive material 414 and seed layer 411 have the grain size mentioned hereinabove.

FIG. 4E illustrates the manner in which a plurality of the layers of the stack 400  
20 are removed by chemical-mechanical polishing, in accordance with operation 468 of FIG.

4. In particular, the photoresist layer 410, adhesion promoter layer 408, and silicon dielectric layer 406 are removed. As shown, the polishing results in a coil structure 422 with a planar surface.

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- 13 -



# CLAIMS

What is claimed is:

- 1 I. A process for manufacturing a coil structure for a magnetic head, comprising:
  - 2 depositing an insulating layer;
  - 3 depositing a photoresist layer on the insulating layer;
  - 4 depositing a silicon dielectric layer on the photoresist layer;
  - 5 masking the silicon dielectric layer;
  - 6 etching a plurality of channels in the photoresist layer and the silicon dielectric
  - 7 layer;
  - 8 depositing a conductive seed layer in the channels;
  - 9 filling the channels with a conductive material to define a coil structure; and
  - 10 chemical-mechanical polishing the conductive material for the planarizing
  - 11 thereof.

SUN

P.L.  
OLE

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Z.H.  
DT

- 1 2. The process as recited in claim 1, wherein the insulating layer includes  $Al_2O_3$ .

Z.H.

SUN PPN

P.L.  
OLE

- 1 3. The process as recited in claim 1, wherein the conductive seed layer includes Cu.

PPN SUN PPN

P.L.  
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- 1 4. The process as recited in claim 1, wherein the conductive material includes Cu.

Z.H.

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P.L.

OLE

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- 17 -

- 1 5. The process as recited in claim 1, wherein a grain size of the conductive material  
2 is less than half of a smallest dimension of the channels.
- 1 6. The process as recited in claim 1, wherein a resistivity of the conductive seed  
2 layer is less than or equal to 8.3 micro-ohm/cm.
- 1 7. The process as recited in claim 1, wherein the silicon dielectric layer includes  
2 SiO<sub>2</sub>.
- 1 8. The process as recited in claim 1, wherein the channels include a slope less than  
2 one (1) and greater than zero (0).
- 1 9. The process as recited in claim 1, wherein the slope of the channels facilitate the  
2 depositing of the conductive seed layer and the conductive material.
- 1 10. The process as recited in claim 1, wherein an aspect ratio of the channels is at  
2 least 7.
- 1 11. The process as recited in claim 1, wherein the masking includes depositing  
2 another photoresist layer.

SVN  
R.H. PLE PPN

PRW SVN  
PLE  
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Z.H. PLE PPN

Z.H. SVN  
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Z.H. SVN  
PLE PPN

R. Fecce  
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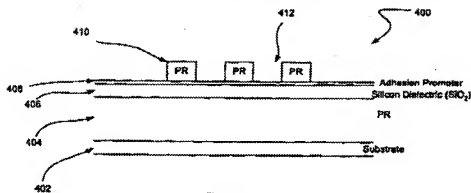


FIG. 4A

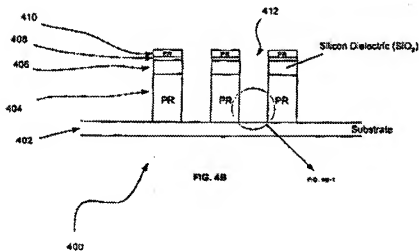


FIG. 4B

R. Feece  
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